(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 271 246 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.01.2003 Bulletin 2003/01

(51) Int Cl.7: G03F 7/20, H01L 21/66

(21) Application number: 01114670.1

(22) Date of filing: 19.06.2001

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant: Infineon Technologies AG
81669 München (DE)

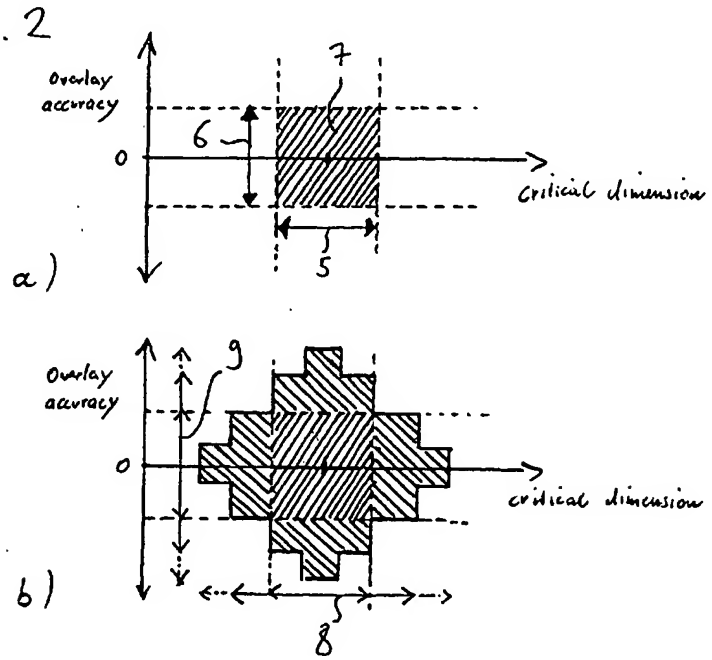
(72) Inventors:
- Schedel, Thorsten
01109 Dresden (DE)
- Schmidt, Sebastian
01127 Dresden (DE)
- Zimmermann, Jens
01465 Langebrück (DE)

(74) Representative: Epping Hermann & Fischer
Ridlerstrasse 55
80339 München (DE)

(54) Method for monitoring the quality of a lithographic structuring step

(57) After exposure of a semiconductor wafer (1) quality parameters (3) like critical dimension, overlay accuracy, alignment parameters etc. are measured in successive inspections and compared with tolerance ranges (9) being specified dynamically by calculating the range from measured values of one or more of the other quality parameters (2). E.g., the tolerance range (9) for overlay accuracy can be increased for smaller measured critical dimension values of the same structures without affecting the functionality of the integrated circuit. By means of a forward mechanism the tolerance ranges can also be adjusted with quality parameter (2) measurements from a first layer to the quality parameter (3) tolerance range (9) of a second layer.

Fig. 2



EP 1 271 246 A1

Description

[0001] The present invention relates to a method for controlling the quality of a lithographic structuring step performed in an exposure tool for structuring a pattern into a photoresist layer of a semiconductor wafer, said quality being represented by a group of at least two quality parameters measured in at least one metrology tool.

[0002] Semiconductor wafers commonly experience multiple exposure steps followed by other processing steps like etching, polishing, etc. in order to be finally structured with one or more integrated circuits. Due to the steadily increasing customer specifications that have to be fulfilled, each exposure step is controlled for its quality performance by a set of metrology measurements.

[0003] The quality of an exposure step can be represented by a group of quality parameters like critical dimension, overlay accuracy from layer to layer, layer thickness, absolute position accuracy (registration), etc. The strength of the requirements to be fulfilled by an integrated circuit, i. e. wafer, typically depend on the layer that is actually being structured. For example, some layers are structured with dense patterns, such that narrow tolerance ranges for the critical dimension exist. In other cases, two subsequent layers, one being structured above the other, require a minute adjustment to each other to provide contacts having a minimum cross-section in order to guarantee an accurate working function of the integrated circuit.

[0004] A set of tolerance specifications for said quality parameters are commonly deduced from the design rules and layer architecture combined with current technology feasibilities. The specifications are generally provided prior to starting mass production of wafers in a fabrication facility. That is, each of the metrology tools measuring at least one of the quality parameters is connected to a product database containing the pattern design files. The quality check, i. e. the comparison whether the just measured quality parameter is within the prescribed tolerance range for that parameter, is performed either on the metrology tool after having received the tolerance specification information, or after transferring its measured values to the MES-system (manufacturing execution system), which performs electronic data collection.

[0005] Unfortunately, the amount of rework is growing with the advent of tighter tolerance specifications introduced with advanced technologies. This is due to a wafer, which does not fulfil the specified tolerances with its measures values, must be reworked, i.e. the resist has to be stripped off, and a new coating step has to be performed after which the wafer is re-exposed. This disadvantageously increases the costs in material and tool time as well as a loss in yield. A remedy would be to decrease the strength of tolerance specifications, but this will lead to a disadvantageous loss in competitiveness to other manufacturers.

[0006] It is therefore a primary objective of the present invention to reduce the amount of rework, thereby decreasing the costs related to exposing a semiconductor wafer.

[0007] The objective is solved by a method for controlling the quality of a lithographic structuring step performed in an lithographic structuring tool for structuring a pattern into a layer of a semiconductor wafer, said quality being represented by a group of at least two quality parameters measured in at least one metrology tool, comprising the steps of transferring a value, or a range of values, of at least a first quality parameter to said metrology tool, calculating a tolerance range for a second quality parameter of said structured pattern in response to said comparison, providing said semiconductor wafer to said metrology tool, performing a measurement of said second quality parameter, comparing said measured quality parameter with said calculated tolerance range.

[0008] The method is particularly advantageous in the case of the plate-like object being a semiconductor device, e.g. a semiconductor wafer, and the lithographic tool being an exposure tool, e.g. a wafer scanner or stepper, or an x-ray, EUV-, ion or electron beam projection tool. It is also considered, that an etching tool can be used as a structuring tool to apply the process window handling method according to the present invention.

[0009] The plate-like object can be any object, which can be structured on its surface, e.g. a mask or reticle, or a flat panel display.

[0010] According to the present method, the quality parameters being measured subsequently in one, two, three or more metrology tools after the exposure of a semiconductor wafer are checked for validity in dependence from the respectively other measurement results. This means that the measurement result of a first measured quality parameter has an influence on the tolerance specification for the second or any further quality parameter being measured afterwards, or even prior to the current measurement, when the validity check of the first quality parameter is taken a posteriori.

[0011] In prior art, each quality parameter such as critical dimension, overlay accuracy, layer thickness, position accuracy, or alignment parameters like grid scaling, magnification, rotation, etc. - the latter ones being derived, e.g., in overlay metrology tools - are each compared against a specific tolerance range specified in advance of wafer production start. Instead of using these rigidly set tolerance ranges, the present method provides a flexible use of ranges, which utilizes advantageously conditions, which are fulfilled by a first measured quality parameter in order to adjust the tolerance range, which is applied to the validity check of the second measured quality parameter.

[0012] The advantage of the present method derives from the physical or geometrical interdependence of the me-

trology or quality parameters involved. A specific value measured for one parameter can have direct influence on the degree of freedom of another parameter. For example, an increased value of critical dimension of a structure might increase a tolerance of overlay accuracy for a contact hole to which it should be connected, or vice-versa decreases the tolerance range for a structure that is to be placed directly besides the first structure, if they are supposed not to be connected. Therefore, data of actually structured patterns - perhaps in combination with design data - are used as input to deriving tolerance ranges instead of using design data only.

[0013] Since the dynamic determination of the tolerance range of the second quality parameter allows an adaption of the quality check to current and actual requirements of design patterns on the wafer under investigation, the dynamic tolerance ranges will generally be larger than those specified rigidly according to prior art. In particular, the process window in a quality parameter plane can be extended into regions, where the functionality of the integrated circuit can still be warranted depending on the specific combination of values for the first and second quality parameter. Thus, rework is advantageously reduced, thereby decreasing costs needed for material and machines.

[0014] The method according to the present invention works with any sequence of measuring quality parameters. Typically, semiconductor wafers will be taken from the lithography track after exposure and the overlay control is measured first, followed by a critical dimension measurement, or vice versa. Then, the wafer may be deposited back on the track for further processing if both or more measurements of parameters values lie within the calculated tolerance ranges. Since according to this method a larger space of valid parameter combinations, i.e. pairs or triples etc., of measured quality parameters that fulfil the tolerance ranges being specified and calculated, respectively, semiconductor wafers, which in prior art methods would be sent into rework due to excessive parameter values, might now pass the examination successfully. This is due to the calculation step which can be chosen to consider all relevant requirements inferred from the design and combined with data from actually built structures.

[0015] The present method is not necessarily restricted to first measuring a first quality parameter that is measured and compared with a rigidly set tolerance range, after which the present method is applied with the calculated tolerance range for performing the second comparison. Rather, it is also possible to perform both measurements for both parameters, and then transferring the measured values for the quality parameters to the respectively other tool, i.e. exchanging the values. Thereby, the method is applied to each of the tools with respect to the semiconductor wafer under investigation. The calculation step is then performed in response to the transferred/exchanged complementary parameter value.

[0016] Generally, it is also possible that the transferred quality parameter value is not measured but derived by statistical means, e. g. mean values derived from a lot to which the semiconductor wafer belongs.

[0017] In a further aspect, an error signal is considered to be issued if the quality parameter, which is measured at second, third, fourth, etc. place, exceeds the tolerance range which has been calculated according to the method. The signal can be forwarded to the host of the corresponding metrology tool, thereby warning the operator about the occurrence of an examination failure, or the signal can be transferred to the fabrication-wide electronic data collection system, which allows further data analysis.

[0018] As a result of this, a rework operation can be performed on a semiconductor wafer, when the measured value exceeds the dynamically determined tolerance range.

[0019] In a further aspect, it is considered that the dynamic specification leading to the calculated tolerance range retrieves its informational input from the design rules corresponding to the current product. Nevertheless, fine tuning of the tolerance range can also be performed with input from experimental data using test wafers varying focus exposure and alignment parameters, thereby scanning the focus parameter and alignment parameter range in a matrix form.

[0020] In a further aspect, the first quality parameter is considered to be derived by a first measurement in a first metrology tool, thereby possibly being checked against a specified rigid tolerance range. The measured value of the first quality parameter may then be transferred to the second metrology tool measuring the second quality parameter after performing the tolerance range calculation, or is transferred to the fabrication-wide electronic data collection system for performing the calculation step. In a further aspect, the first quality parameter is considered to be the critical dimension of said pattern. In combination with a still further aspect, the second quality parameter being the overlay accuracy of two recent layers, the method becomes particularly advantageous. As stated in a previous example, the critical dimension and the overlay accuracy have a strong interrelation with respect to obeying old design rules.

[0021] Nevertheless, in two further aspects, the first and second quality parameters are considered to measure the same quality. In a first of those aspects, the first quality parameter is measured in a first layer and the second quality parameter is measured in a second layer, which is different from the first layer. This aspect of the method according to the present invention advantageously can be applied to the common case that two, e.g., subsequent layers comprise a structure design, which depends on each other. Thus, if a quality parameter in one of these layers acquires a first value by measurement, the second quality parameter measuring the same quantity of the corresponding structure in the layer above, can advantageously be compared with a tolerance range determined and calculated from conditions of the corresponding structure below. For example, a poorly structured pattern in the lower layer, i. e. a measured first quality parameter slightly exceeding the rigid tolerance range specified according to prior art, can be remedied by an

accurately structured second quality parameter, such that the pattern providing the integrated circuit is not damaged design rule violation.

[0022] The other of the two aspects considers the same quantity to be measured in an x- and y-direction. An example would be a structure that has to fulfil overlay conditions like a minimum cross-section with a different second structure in an underlying layer, and the quality parameters are: overlay accuracy each in x- and y-direction. If the second structure to be overlaid by the current structure of which the parameters are to be derived and measured, has a structure boundary extending in a diagonal form across its layer, it may occur that a misalignment in x-direction can be outweighed by another misalignment in y-direction in order to maintain cross-section validity.

[0023] Further aspects and advantages are evident from the dependent claims.

[0024] The invention will be better understood by reference to embodiments taken in conjunction with the accompanying drawings, wherein

Figure 1 shows a contact hole having an overlay in accuracy, which is etched between two gate electrodes with a small (a) and large (b) critical dimension,

Figure 2 shows the process window of tolerance ranges with respect to overlay accuracy and critical dimension as specified in rigid form according to prior art (a), and as specified dynamically with a tolerance range of a first parameter being a function of the second parameter,

Figure 3 displays a flow chart of the method according to the present invention.

[0025] The interrelation between quality parameters due to the requirement of a non-violation of the design pattern function is illustrated in figure 1. There, a semiconductor wafer 1, which has arrived at a processing status of filling the contact holes 20 being etched towards the substrate between two gate electrodes of a DRAM-pattern (Dynamic Random Access Memory). The gate electrodes 21 are protected by liners, such that a contact between said contact hole 20 and said gate electrode 21 is prohibited. Nevertheless, a sufficient cross-section of the contact hole filled, e. g., with poly-silicon must exceed a minimum value in order to establish a contact to the bit line for accessing the capacitor current information.

[0026] A contact hole 20 having a comparatively small critical dimension and a moderate amount of overlay accuracy 3 is shown in figure 1a. From this figure, it becomes clear that the requirement of a minimum cross-section, i. e. the bottom section of contact hole 20, admits a complicated space in a plane given by critical dimension 2 and overlay accuracy 3. If, e. g., the critical dimension 2 is increased as shown in figure 1b the cross-section priorily increases but half of the contact hole extent is ineffective due to covering the gate electrode 21.

[0027] Moreover, if the overlay accuracy 3 also reveals a larger value of deviation, the cross-section even further decreases. This could be outweighed by an even larger critical dimension 2, as long as the contact hole extent does not lead to other relevant design problems, for example contacting other lines or contact holes.

[0028] The following table gives an example of a specification derived from a gate layer measurement:

case	gate measurement range CD	contact tolerance range CD
a	130 nm - 150 nm	180 nm - 240 nm
b	150 nm - 170 nm	190 nm - 230 nm

[0029] Accordingly, a gate electrode critical dimension measurement of 152 nm leads to a specification tolerance for the corresponding critical dimension of a contact hole in the range 190 nm - 230 nm. In this context, critical dimension measurements of two different layers also define a measure for their respective overlay accuracy to some degree.

[0030] Similarly, an overlay accuracy can be provided directly from a critical dimension (CD) measurement:

Case	contact hole measurement range CD	contact hole tolerance range of overlay accuracy
a	180 nm - 200 nm	90 nm
b	200 nm - 220 nm	80 nm
c	220 nm - 240 nm	70 nm

[0031] E.g., a measured critical dimension of a contact hole of 191 nm (case a) leads to an overlay tolerance range of 90 nm, which provides a broader range, than if a larger critical dimension would have been measured.

[0032] The prior art approach to specify conditions, i.e. tolerance ranges for each of the parameters, critical dimension 2 and overlay accuracy 3, is shown in figure 2a. The rigidly specified tolerance ranges 5, 6 being independent from

each other leave behind just a small space of quality parameter combinations, i. e. pairs of e. g. critical dimension 2 and overlay accuracy 3, not taking into account dynamically produced situations where the requirement of an operational integrated circuit might be fulfilled although at least one of the limits of the tolerance ranges 6, 7 are violated.

[0033] A set of two tolerance ranges 8, 9 each being a function of a complementary quality parameter, e. g. the tolerance range 8 for critical dimension 2 as a function of overlay accuracy 3, is shown in figure 2b. Advantageously, a larger space of quality parameter combinations as compared with prior art is found to be provided depending on the design and the actual exposure quality.

[0034] The dynamically determined process window as illustrated in figure 2b can be calculated according to the embodiment of the method of the present invention as shown in the flow chart of figure 3, where only the section of the overlay measurement is shown. After exposure, a semiconductor wafer 1 is first measured for the critical dimension at specific measurement marks. A semiconductor wafer 1 is then forwarded from the optical microscope performing this task to an overlay tool. The host computer of said overlay tool sends a request for the measured critical dimension value, which is attached to the wafer 1 in an EDC-database being accessible fab-wide, or directly from the optical microscope.

[0035] The overlay tool host also acquires design data and builds up a model of the three-dimensional pattern under investigation to which the actually measured critical dimension data is added. Boundary conditions that are to be fulfilled, like minimum requirements for contact cross-sections or minimum line-to-line distances, etc. are considered when calculating dynamically a tolerance range for the overlay accuracy. Thus, the overlay accuracy tolerance range particularly depends on the measured value of the critical dimension as provided by the optical microscope according to this embodiment.

[0036] In the meantime, the overlay accuracy is measured by the overlay tool and the corresponding value is compared with the overlay tolerance range 9 as just derived from the critical dimension 2. In case the comparison reveals a tolerance limit violation, an error signal 10 is issued leading the operator to initiate a rework operation for the semiconductor wafer 1. Alternatively, the semiconductor wafer 1 is forwarded to the next process step, e. g. developing the resist that previously has been exposed.

[0037] According to figure 2b, the measured overlay accuracy could also be transferred back to an optical microscope host for a posteriori calculating a dynamic tolerance range 8 out of the provided overlay accuracy. A further error signal can then be issued signaling that the corresponding tolerance range limit has been violated.

[0038] According to another embodiment relating to memory products as an example quality parameters can be calculated from two suited specification parameters s1, s2, which are more abstract than those, which can be measured directly: consider

$$s1 = cd1 + cd3 + ovl$$

$$s2 = cd1 / 2 + cd2 + cd3 / 2 ,$$

where cd1 is the width of a structure corresponding to an active area, which extends between two deep trenches having a width cd3. Both structures overlap with a width ovl, measured in the same direction as cd1 and cd3. There is also a distance cd2 measuring the distance between said active area and a further deep trench. s1 and s2 are to be specified with rigid tolerance ranges, but are used for determining dynamic ranges 8, 9 of the quality parameters cd1, cd2, cd3, ovl in this example. In particular a larger deviation from the ideal value of measured deep trench width cd3 requires tighter specification for cd1 and overlay ovl. Therefore s1 and s2 can be used as a formula for performing the calculation step.

List of references

[0039]

1 semiconductor
2 first quality parameter, critical dimension
3 second quality parameter, overlay accuracy
5 first tolerance range, rigid
6 second tolerance range, rigid
7 valid quality parameter space
8 first tolerance range, dynamically specified
9 second tolerance range, dynamically specified

10 error signal
20 contact hole, contact bit line
21 gate electrode, gate contact

Claims

1. Method for controlling the quality of a lithographic structuring step performed in a lithographic structuring tool for structuring a pattern into a layer of a plate-like object (1), said quality being represented by a group of at least two quality parameters, the first quality parameter (2) being measured in a first metrology tool and the second quality parameter (3) being measured in a second metrology tool, the first and second quality parameters (2, 3) representing different properties of the pattern, comprising the steps of:

   - providing at least one value of a first quality parameter (2) of said plate-like object (1),
   - calculating a tolerance range for a second quality parameter (3) of said structured pattern in response to said providing said at least one value,
   - providing said semiconductor wafer (1) to said second metrology tool,
   - performing a measurement of said second quality parameter (2) in said second metrology tool,
   - comparing said measured second quality parameter (2) with said calculated tolerance range (9).

2. Method according to claim 1,
   characterized in that

   - said lithographic structuring tool is an exposure tool,
   - said lithographic structuring step is an exposure step,
   - said plate-like object is a semiconductor wafer (1),
   - said layer is a photoresist layer.

3. Method according to claim 2,
   characterized in that
   an error signal (10) is issued, if said second quality parameter (3) exceeds said tolerance range (9).

4. Method according to claim 3,
   characterized in that
   said exposure step is repeated in response to said error signal (10).

5. Method according to claim 1,
   characterized in that
   said calculation of said tolerance range (9) is performed by using pattern design data.

6. Method according to claim 1,
   characterized in that
   said value of said first quality parameter (2) is provided by

   - providing said semiconductor wafer (1) to said first metrology tool,
   - performing a measurement of said first quality parameter (2) using said first metrology tool,

   prior to being transferred to the second metrology tool, which measures the second quality parameter (3).

7. Method according to claim 6,
   characterized by

   - defining a first tolerance range (8) for a first quality parameter (2) of said structured pattern prior to said measurement of said first quality parameter (2),
   - comparing said measured first quality parameter (2) with said first tolerance range (8),
   - issuing an error signal, if said first quality parameter (2) exceeds said first tolerance range (8).

8. Method according to anyone of claims 1 to 7,

characterized in that
said first quality parameter (2) represents the critical dimension of said pattern.

9. Method according to anyone of claims 2 to 7,
characterized in that

- said photoresist layer represents at least a second layer structured on said semiconductor wafer (1),
- said second quality parameter (3) represents an overlay accuracy of said pattern with respect to a pattern designed to have received the same position in a previous exposure step in another layer of said semiconductor wafer (1).

10. Method according to claim 8,
characterized in that

- said first (2) and second quality parameter (3) represent the same quantity,
- said first quality parameter (2) is measured in a layer, which is structured prior to said exposure step.

11. Method according to claim 8,
characterized in that

- said first (2) and second quality parameter (3) represent the same one-dimensional quantity,
- said first quality parameter (2) is measured in a first direction of a layer,
- said second quality parameter (3) is measured in a second direction of a layer, which is perpendicular to said first direction,

12. Method according to anyone of claims 1 to 11,
characterized in that
said first quality parameter (2) is provided to said second metrology tool, which measures said second quality parameter (3), and said calculation is performed at said second metrology tool.

13. Method according to claim 1,
characterized in that
said plate-like object (1) is a flat panel display.

Fig. 1

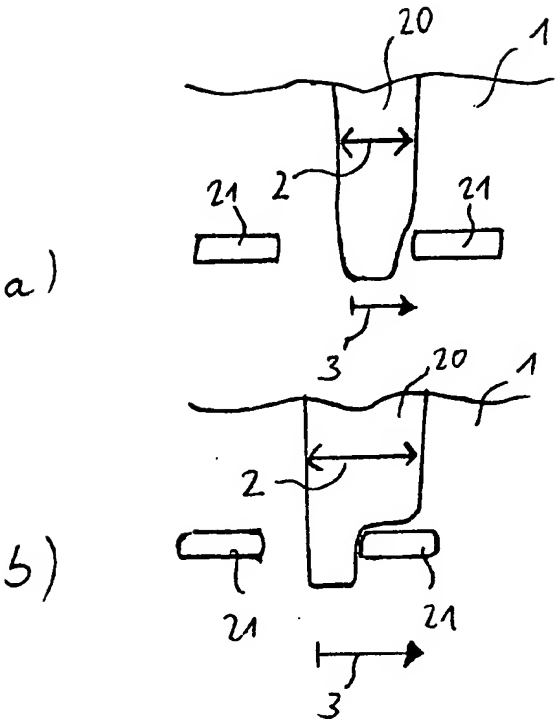

20
1
21
2
21
a)
3
20
1
2
b)
21
21
3

Fig. 2

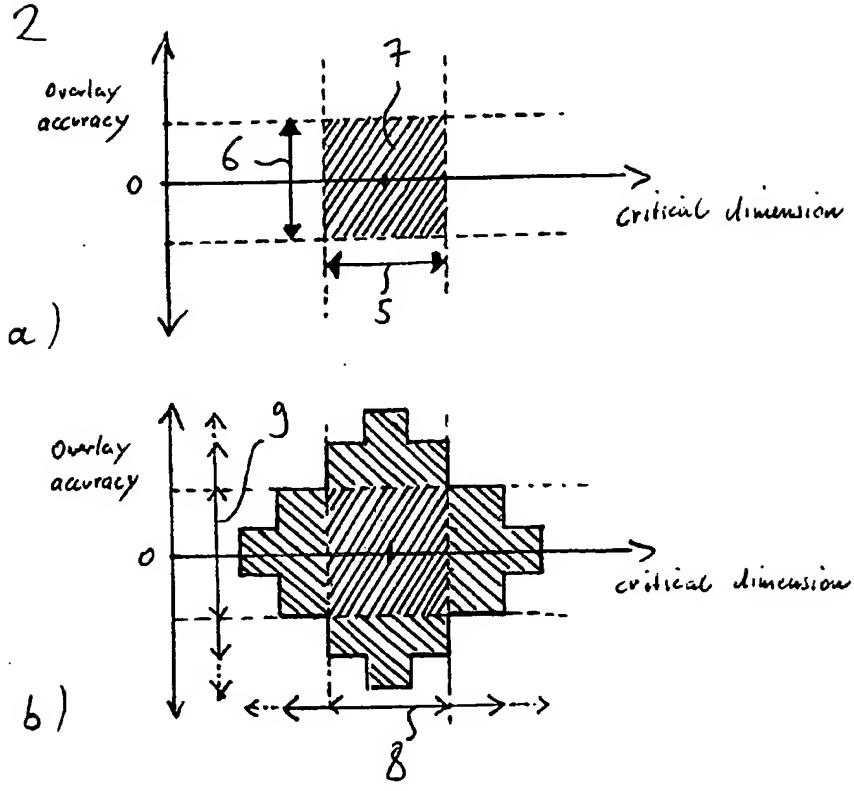
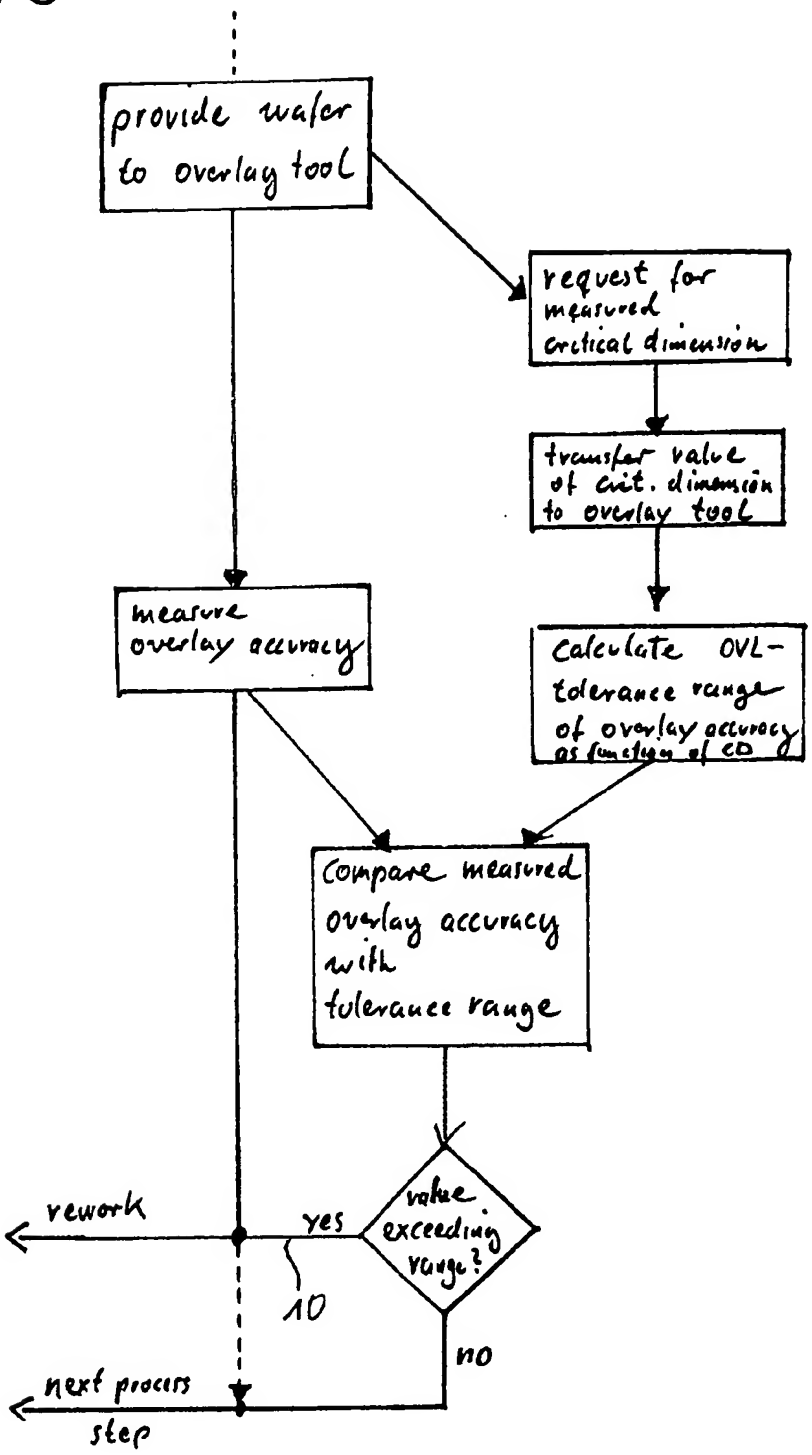

Overlay accuracy
7
6
0
critical dimension
5
a)
Overlay accuracy
9
0
critical dimension
b)
8

Fig. 3


provide wafer to overlay tool
request for measured critical dimension
transfer value of crit. dimension to overlay tool
measure overlay accuracy
calculate OVL-tolerance range of overlay accuracy as function of CD
compare measured overlay accuracy with tolerance range
value exceeding range?
yes
rework
10
no
next process step

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 11 4670

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 790 254 A (AUSSCHNITT CHRISTOPHER PERRY) 4 August 1998 (1998-08-04) * column 1, line 14 - line 16 * * column 5, line 8 - column 8, line 13 * * figures 9-11,13 *	1-13	G03F7/20 H01L21/66
X	US 5 866 437 A (CHEN MING CHUN ET AL) 2 February 1999 (1999-02-02) * column 3, line 27 - column 4, line 11 * * figures 2,3 *	1-13	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G03F
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 December 2001	Heryet, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 11 4670

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

21-12-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5790254 A	04-08-1998	US 5629772 A WO 9849538 A1	13-05-1997 05-11-1998
US 5866437 A	02-02-1999	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82